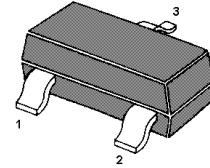
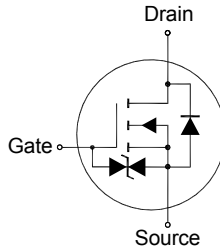


# MMBT7002K

## N-Channel Enhancement Mode Field Effect Transistor

### Features

- Low on resistance  $R_{DS(ON)}$
- Low gate threshold voltage
- Low input capacitance
- ESD protected up to 2KV



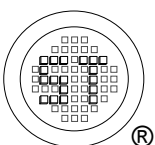
1. Gate 2. Source 3. Drain  
TO-236 Plastic Package

### Absolute Maximum Ratings ( $T_a = 25\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	60	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (Continuous)	$I_D$	300	mA
Drain Current (Pulse Width $\leq 10\text{ }\mu\text{s}$ )	$I_{DM}$	800	mA
Total Power Dissipation	$P_{tot}$	350	mW
Operating and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$

### Characteristics at $T_a = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Min.	Max.	Unit
Drain Source Breakdown Voltage at $I_D = 10\text{ }\mu\text{A}$	$BV_{DSS}$	60	-	V
Zero Gate Voltage Drain Current at $V_{DS} = 60\text{ V}$	$I_{DSS}$	-	1	$\mu\text{A}$
Gate Source Leakage Current at $V_{GS} = \pm 20\text{ V}$	$I_{GSS}$	-	$\pm 10$	$\mu\text{A}$
Gate Threshold Voltage at $V_{DS} = 10\text{ V}, I_D = 250\text{ }\mu\text{A}$	$V_{GS(th)}$	1	2.5	V
Static Drain Source On-Resistance at $V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$ at $V_{GS} = 4.5\text{ V}, I_D = 200\text{ mA}$	$R_{DS(ON)}$	- -	3 4	$\Omega$
Forward Transconductance at $V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$	$g_{fs}$	80	-	mS
Input Capacitance at $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	$C_{iss}$	-	50	pF
Output Capacitance at $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	$C_{oss}$	-	25	pF
Reverse Transfer Capacitance at $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	$C_{rss}$	-	5	pF



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ISO14001 : 2004  
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Certificate No. 7116



IECQ QC 080000  
Certificate No. PRC-HSPM-1485-1

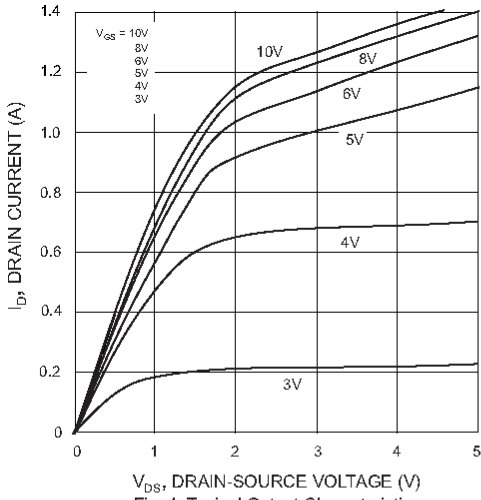


Fig. 1 Typical Output Characteristics

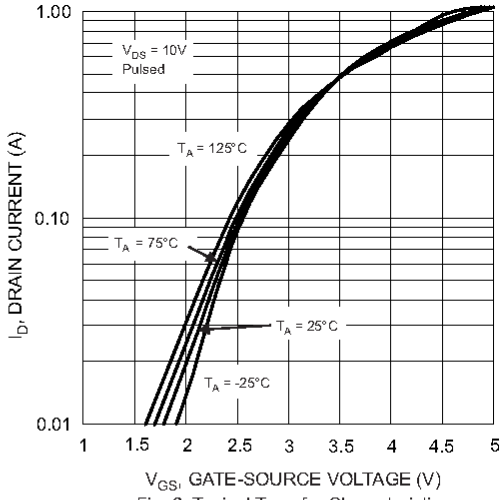


Fig. 2 Typical Transfer Characteristics

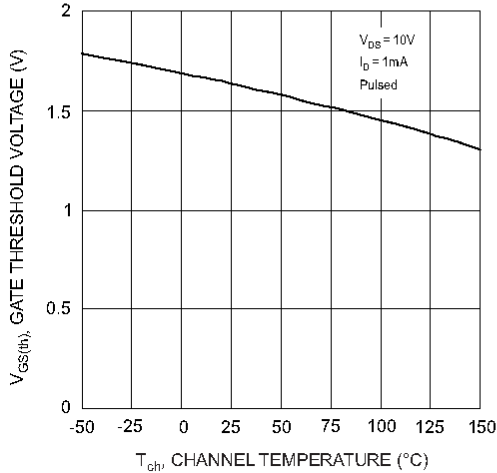


Fig. 3 Gate Threshold Voltage vs. Channel Temperature

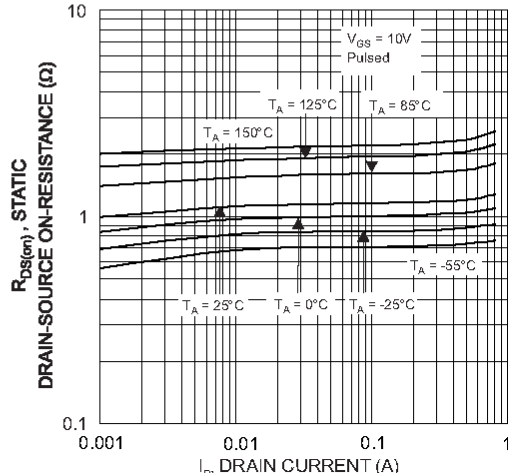


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

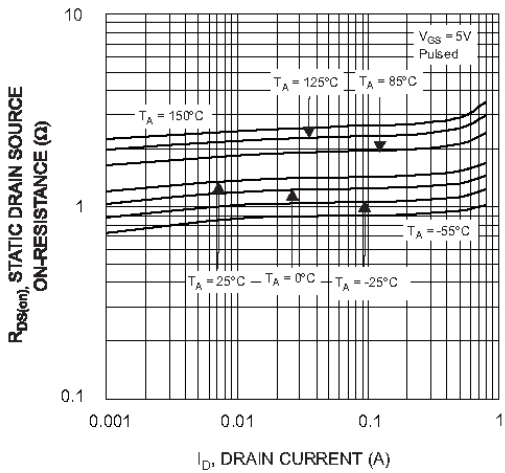


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

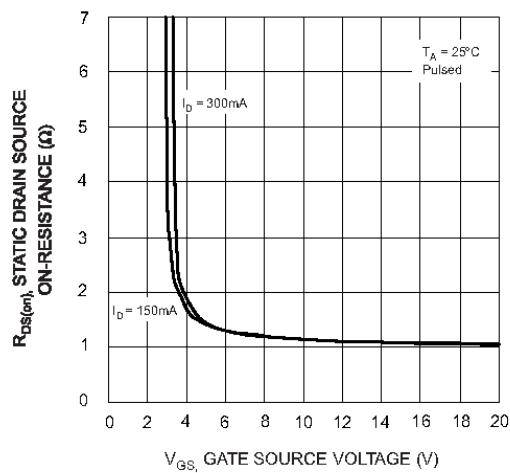
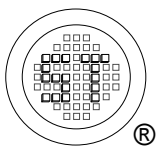


Fig. 6 Static Drain-Source On-Resistance vs. Gate-Source Voltage



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